AMENDMENTS

Please amend the above-identified application as follows:

In the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

1. (Currently Amended) An apparatus for performing correctness 1 checks, the apparatus comprising: 2 logic configured to receive a first set of instructions; and 3 logic configured to generate an initial instruction schedule and a conditional 4 instruction stream from the first set of instructions, such that the initial instruction 5 schedule is devoid of code sequences comprising correctness check functions and 6 such that code sequences of the conditional instruction stream are associated with a 7 8 corresponding set of one or more instructions in the initial instruction schedule the first set of instructions including one or more instructions associated with a 9 10 correctness check function associated with a particular portion of the first set of instructions, the correctness check function configured to evaluate at least one of a 11 value, a range of values, and a relationship between values after execution of the 12 particular portion of the first set of instructions; 13 logic configured to evaluate the initial instruction schedule to determine 14 whether the initial instruction schedule includes spare instruction slots into which said 15 one or more instructions code sequences associated with the correctness check 16 17 functions can be inserted into the initial instruction schedule such that a final instruction schedule responsive to the initial instruction schedule would not require a 18 longer run time than the initial instruction schedule; and 19 logic configured to generate the final instruction schedule responsive to the 20 21 initial instruction schedule, the conditional instruction stream, and the logic configured to evaluate insert said one or more instructions associated with the 22 correctness check function into the spare instruction slots if enough spare instruction 23 24 slots exist in the initial instruction schedule for accommodating said one or more instructions. 25

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1	2. (Currently Amended) The apparatus of claim 1, wherein said
2	one or more instructions associated with the correctness check function correspond to
3	a conditional expression, and wherein the first logic performs initial code generation
4	prior to generating the initial instruction schedule, wherein when the first logic
5	performs initial code generation, said one or more instructions associated with the
6	correctness check function are separated from all other instructions of said first set o
7	instructions so that the initial instruction schedule does not include any instructions
8	associated with the correctness check function correctness check functions are
9	configured to evaluate at least one of a value, a range of values, and a relationship
0	between values after execution of the corresponding instructions in the initial
1	instruction schedule.
1	3. (Currently Amended) The apparatus of claim 2 1, wherein sai
2	logic configured to generate an initial instruction schedule and a conditional
3	instruction stream from the first set of instructions is responsive to an input provided
4	to a compiler first, second and third logic correspond to a processor programmed to

logic configured to generate an initial instruction schedule and a conditional instruction stream from the first set of instructions is responsive to an input provided to a compiler first, second and third logic correspond to a processor programmed to execute a compiler program, the compiler program including a first code segment for performing initial code generation and for generating the initial instruction schedule, a second code segment for evaluating the initial instruction schedule to determine whether spare instruction slots exist in the initial instruction schedule, and a third code segment for inserting said one or more instructions associated with the correctness check function into the spare instruction slots if enough spare instruction slots exist to accommodate said one or more instructions.

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4. (Currently Amended) An apparatus for performing correctness 1 checks, the apparatus comprising: 2 means for receiving a first set of instructions; and 3 means for generating an initial instruction schedule and a conditional 4 instruction stream from the first set of instructions, such that the initial instruction 5 schedule is devoid of code sequences comprising correctness check functions and 6 such that code sequences of the conditional instruction stream are associated with a 7

corresponding set of one or more instructions in the initial instruction schedule the

9 first set of instructions including one or more instructions associated with a

correctness check function associated with a particular portion of the first set of instructions, the correctness check function configured to evaluate at least one of a value, a range of values, and a relationship between values after execution of the particular portion of the first set of instructions;

means for evaluating the initial instruction schedule to determine whether the

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means for evaluating the initial instruction schedule to determine whether the initial instruction schedule includes spare instruction slots into which said one or more instructions code sequences associated with the correctness check functions can be inserted into the initial instruction schedule such that a final instruction schedule would not require a longer run time than the initial instruction schedule; and

means for inserting said one or more instructions code sequences associated with the correctness check function into the spare instruction slots if enough spare instruction slots exist in the initial instruction schedule for accommodating said one or more instructions code sequences.

- 5. (Currently Amended) The apparatus of claim 4, wherein said one or more instructions associated with the correctness check function correspond to a conditional expression, and wherein the first means performs initial code generation prior to generating the initial instruction schedule, wherein when the first logic performs initial code generation, said one or more instructions associated with the correctness check function are separated from all other instructions of said first set of instructions so that the initial instruction schedule does not include any instructions associated with the correctness check function correctness check functions are configured to evaluate at least one of a value, a range of values, and a relationship between values after execution of the corresponding instructions in the initial instruction schedule.
- 6. (Currently Amended) A method for performing correctness checks, the method comprising the steps of:
 receiving a first set of instructions; and
 generating an initial instruction schedule and a conditional instruction stream
 from the first set of instructions, such that the initial instruction schedule is devoid of code sequences comprising correctness check functions and such that code sequences of the conditional instruction stream are associated with a corresponding set of one or

more instructions in the initial instruction schedule the first set of instructions including one or more instructions associated with a correctness check function associated with a particular portion of the first set of instructions, the correctness check function configured to evaluate at least one of a value, a range of values, and a relationship between values after execution of the particular portion of the first set of instructions;

evaluating the initial instruction schedule to determine whether the initial

evaluating the initial instruction schedule to determine whether the initial instruction schedule includes spare instruction slots into which said one or more instructions code sequences from the conditional instruction stream and associated with the correctness check functions can be inserted into the initial instruction schedule such that a final instruction schedule would not require a longer run time than the initial instruction schedule; and

inserting said one or more instructions code sequences associated with the correctness check function into the spare instruction slots if enough spare instruction slots exist in the initial instruction schedule for accommodating said one or more instructions code sequences.

- 7. (Currently Amended) The method of claim 6, wherein evaluating the initial instruction schedule comprises comparing the run time length of one or more spare instruction slots with the run time length of a code sequence associated with a corresponding portion of the initial instruction schedule said one or more instructions associated with the correctness check function correspond to a conditional expression, and wherein the step of generating the initial instruction schedule includes the step of performing initial code generation, wherein when initial code generation is performed, said one or more instructions associated with the correctness check function are separated from all other instructions of said first set of instructions so that the initial instruction schedule does not include any instructions associated with the correctness check function.
- 8. (Currently Amended) The method of claim 7 6, wherein evaluating the initial instruction schedule further comprises discarding code sequences having a run time length greater than the run time of one or more spare instruction slots associated with a corresponding portion of the initial instruction schedule the

method is performed by a processor programmed to execute a compiler program, the compiler program including a first code segment for performing initial code generation and for generating the initial instruction schedule, a second code segment for evaluating the initial instruction schedule to determine whether spare instruction slots exist in the initial instruction schedule, and a third code segment for inserting said one or more instructions associated with the correctness check function into the spare instruction slots if enough spare instruction slots exist to accommodate said one or more instructions.

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9. (Currently Amended) A computer program for performing correctness checks, the computer program being embodied on a computer-readable medium, the computer program comprising:

a first code segment configured to receive a set of instructions;

a second code segment configured to generate, the first code segment generating an initial instruction schedule and a conditional instruction stream from a first the set of instructions, such that the initial instruction schedule is devoid of code sequences comprising correctness check functions and such that the code sequences of the conditional instruction stream are associated with a corresponding set of one or more instructions in the initial instruction schedule the first set of instructions including one or more instructions associated with a correctness check function associated with a particular portion of the first set of instructions, the correctness check function configured to evaluate at least one of a value, a range of values, and a relationship between values after execution of the particular portion of the first set of instructions;

a second third code segment, the second code segment configured to evaluate evaluating the initial instruction schedule to determine whether the initial instruction schedule includes spare instruction slots into which said one or more instructions code sequences associated with the correctness check function can be inserted into the initial instruction schedule such that a final instruction schedule would not require a longer run time than the initial instruction schedule; and

a third fourth code segment, the third code segment configured to insert inserting said one or more instructions code sequences associated with the correctness check function into the spare instruction slots if enough when sufficient spare

instruction slots exist in the initial instruction schedule to accommodate said one or more instructions code sequences.

- 10. (Currently Amended) The computer program of claim 9, I wherein said second code segment generates a conditional instruction stream 2 comprising correctness check functions that evaluate at least one of a value, a range of 3 values, and a relationship between values after execution of corresponding 4 instructions in the initial instruction schedule one or more instructions associated with 5 the correctness check function correspond to a conditional expression, and wherein 6 7 prior to generating the initial instruction schedule, the first code segment performs initial code generation, wherein when initial code generation is performed, said one or 8 more instructions associated with the correctness check function are separated from all 9 other instructions of said first set of instructions so that the initial instruction schedule 10 does not include any instructions associated with the correctness check function. 11
- 1 11. (New) The apparatus of claim 1, wherein said logic configured 2 to evaluate the initial instruction schedule discards code sequences within the 3 conditional instruction stream that if inserted into a final instruction schedule would 4 result in a final instruction schedule with a run time greater than a run time of the 5 initial instruction schedule.
- 1 12. (New) The apparatus of claim 1, wherein said logic configured 2 to evaluate the initial instruction schedule identifies code sequences within the 3 conditional instruction stream for insertion into the initial instruction schedule.
- 1 13. (New) The apparatus of claim 12, wherein said logic configured to evaluate the initial instruction schedule identifies code sequences having a length that exceeds the length of a corresponding set of one or more spare instruction slots in the initial instruction schedule.
- 1 14. (New) The apparatus of claim 1, wherein said logic configured 2 to generate the final instruction schedule inserts code sequences associated with

- 3 correctness check functions into spare instruction slots of the initial instruction
- 4 schedule.
- 15. (New) The apparatus of claim 4, wherein said means for
- 2 generating an initial instruction schedule and a conditional instruction stream from the
- 3 first set of instructions is responsive to an input provided to a compiler.